REMARKS

Claims 1-25 are pending in the Application. Claims 1-25 are rejected under 35 U.S.C. §102. Applicants respectfully traverse these rejections for at least the reasons stated below and respectfully request the Examiner to reconsider and withdraw these rejections.

I. REJECTIONS UNDER 35 U.S.C. §102(e):

Claims 1-25 have been rejected under 35 U.S.C. §102(e) as being anticipated by Moran (U.S. Patent No. 6,647,400). Applicants respectfully traverse these rejections for at least the reasons stated below and respectfully request the Examiner to reconsider and withdraw these rejections.

For a claim to be anticipated under 35 U.S.C. §102, each and every claim limitation must be found within the cited prior art reference and arranged as required by the claim. M.P.E.P. §2131.

Applicants respectfully assert that Moran does not disclose "a RAM connected to the bus system, the RAM being divided into pages, each page having an execution flag" as recited in claim 1 and similarly in claims 9 and 18. As understood by the Applicants, the Examiner asserts that Moran inherently discloses the above-cited claim limitation. The Examiner states that the above-cited claim limitation "is considered to [be] include[d] within memory 110." Paper No. 5, page 2. Applicants respectfully traverse the assertion that RAM 110 in Moran is inherently divided into pages where each page has an execution flag. Applicants note that in relying upon the theory of inherency, the Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, in order for the Examiner to establish inherency, the Examiner must provide extrinsic evidence that must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of

ordinary skill. *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). Inherency, however, may not be established by probabilities or possibilities. *Id.* The mere fact that a certain thing may resolve from a given set of circumstances is not sufficient. *Id.* Therefore, the Examiner must support the inherency argument with objective evidence meeting the above requirements. However, the Examiner has not supported her assertion that it is inherent that memory 110 of Moran is divided into pages where each page has an execution flag. Therefore, the Examiner has not presented a *prima facie* case of anticipation for rejecting claims 1, 9 and 18. M.P.E.P. §2131.

Applicants further assert that Moran does not disclose "a memory manager configured to manage the pages of the RAM and permit CPU execution of data on pages according to the execution flag" as recited in claim 1 and similarly in claims 9 and 18. As understood by the Applicants, the Examiner asserts that memory 110 of Moran inherently includes a memory manager configured to manage the pages of the RAM and permit CPU execution of data on pages according to an execution flag. The Examiner states that "a memory manager is considered to [be] include[d] in memory 110 for configuring to manage the pages of the RAM and permit CPU execution of data on pages according to the execution flag." Paper No. 5, page 3. Applicants respectfully traverse the assertion that memory 110 of Moran inherently includes a memory manager configured to manage the pages of the RAM and permit CPU execution of data on pages according to an execution flag. The Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that memory 110 of Moran inherently includes a memory manager configured to manage the pages of the RAM and permit CPU execution of data on pages according to an execution flag. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). As the Examiner has not provided any objective evidence in supporting the assertion that memory 110 of Moran inherently includes a memory manager configured to manage the pages of the RAM and permit CPU execution of data on pages according to an execution flag, the Examiner has not presented a *prima facie* case of anticipation for rejecting claims 1, 9 and 18. M.P.E.P. §2131.

Applicants further assert that Moran does not disclose "wherein the memory manager is configured to determine whether the program is susceptible to buffer overflow attacks, and, if so, set the execution flag for program stack pages of RAM to deny CPU execution of data on the program stack pages of RAM" as recited in claim 1 and similarly in claims 9 and 18. The Examiner cites column 33, lines 64-67; column 34, lines 1-3; and column 34, lines 43-50 of Moran as disclosing the above-cited claim limitation. Paper No. 5, pages 3-4. Applicants respectfully traverse and assert that Moran instead discloses that a SetUID comes from the operating system setting the UID of the command's process to be that of the owner of the file. Column 34, lines 5-7. Moran further discloses that SetUID commands provide restricted access to system resources. Column 34, lines 8-10. Moran further discloses that almost all buffer overflow attacks take effect at the very beginning of the execution of the program, because the data causing the overflow is supplied as part of the command invocation or setup. Column 34, lines 43-46. Moran further discloses that the command is subverted (replaced) before it has a chance to perform any of its intended actions. Column 34, lines 46-48. Moran further discloses that the analysis engine examines the last access time of each SetUID command. Column 34, lines 54-55. Moran further discloses that this access time is compared to the timestamps on files that the command is expected to access. Column 34, lines 60-61. Moran further discloses that if those timestamps are earlier than the last-access time on the SetUID command, this is evidence that a SetUID buffer overflow attack may have occurred. Column 34, lines 61-64. Hence, Moran discloses a description of an overflow buffer attack and a method of detecting whether an overflow attack may have occurred by comparing the last-access time of each SetUID command with the timestamps on files that the command is expected to access. As stated above, the Examiner has not provided any objective evidence that memory 110 includes a memory manager. Further, there is no language in the cited passage as disclosing that a memory manager is configured to determine whether a program is susceptive to buffer overflow attacks. Instead, Moran discloses a method of detecting whether a buffer overflow attack may have occurred. Further, there is no language in the cited passage of setting an execution flag to deny CPU execution of data on the program

stack pages of RAM. Thus, Moran does not disclose all of the limitations of claims 1, 9 and 18, and thus Moran does not anticipate claims 1, 9 and 18. M.P.E.P. §2131.

Applicants further assert that Moran does not disclose "an application program code comprising a set of codes operable to direct a data processing system to request the memory manager code to establish a program stack within at least one page the RAM" as recited in claim 9. As understood by the Applicants, the Examiner asserts that it is inherent in memory 110 of Moran to perform the above-cited claim limitation. Applicants respectfully traverse the assertion that memory 110 of Moran inherently includes codes to perform the above-cited claim limitation. The Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that memory 110 of Moran inherently includes code to perform the above-cited claim limitation. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). As the Examiner has not provided any objective evidence in supporting the assertion that memory 110 of Moran inherently includes code to perform the above-cited claim limitation, the Examiner has not presented a *prima facie* case of anticipation for rejecting claim 9. M.P.E.P. §2131.

Claims 2-8, 10-17 and 19-25 each recite combinations of features including the above combinations, and thus are not anticipated for at least the above stated reasons. Claims 2-8, 10-17 and 19-25 recited additional features, which, in combination with the features of the claims upon which they depend are not anticipated by Moran.

For example, Moran does not disclose "wherein the memory manager and the CPU are configured to deny CPU execution of data by triggering a hardware interrupt" as recited in claim 2 and similarly in claims 10 and 19. As understood by the Applicants, the Examiner asserts that it is inherent that memory 110 of Moran includes a memory manager which along with CPU 102 are configured to deny CPU execution of data by triggering a hardware interrupt. The Examiner does cite to column 5, lines 43-55 of Moran. Paper No. 5, page 4. However, upon review of the cited passage, there is no language in the cited passage that discloses hardware

interrupts, denying CPU execution or a memory manager. Applicants respectfully traverse the assertion that Moran inherently discloses a memory manager and a CPU configured to deny CPU execution of data by triggering a hardware interrupt. As stated above, the Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that memory 110 of Moran inherently discloses a memory manager and that Moran inherently discloses that a memory manager and a CPU are configured to deny CPU execution of data by triggering a hardware interrupt. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). As the Examiner has not provided any objective evidence for supporting that memory 110 inherently includes a memory manager as well as that Moran inherently discloses that a memory manager and CPU 102 are configured to deny CPU execution of data by triggering a hardware interrupt, the Examiner has not presented a *prima facie* case of anticipation for rejecting claims 2, 10 and 19. M.P.E.P. §2131.

Applicants further assert that Moran does not disclose "a process structure table in data communication with the memory manager, wherein the memory manager comprises an annotation API, wherein the annotation API is configured to annotate within the process structure table the susceptibility of the program to buffer overflow attacks, and wherein the memory manager is configured to make the determination of susceptibility to buffer overflow attacks with reference to the process structure table" as recited in claim 3 and similarly in claims 4-5, 11-12 and 20-21. As understood by the Applicants, the Examiner asserts that the above-cited claim limitations are inherent in Moran using language cited in column 5, lines 43-55 of Moran. Applicants respectfully traverse the assertion that the above-cited claim limitations are inherently disclosed in Moran. Further, upon review of the cited passage, there is no language in the cited passage that discloses a process structure table, a memory manager, an API, and an API configured to annotate within the process structure table the susceptibility of the program to buffer overflow attacks or a memory manager configured to make the determination of susceptibility to buffer overflow attacks with reference to the process structure table. As stated above, the Examiner must provide a basis in fact and/or technical reasoning to reasonably

support the determination that Moran inherently discloses the above-cited claim limitations. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). As the Examiner has not provided any objective evidence supporting her inherency arguments, the Examiner has not presented a *prima facie* case of anticipation for rejecting claims 3-5, 11-12 and 20-21. M.P.E.P. §2131.

Applicants further assert that Moran does not disclose "wherein the program is configured to call the annotation API if the program is susceptible to buffer overflow attacks, the memory manager is configured to determine susceptibility upon a request to allocate an additional page of RAM for the program" as recited in claim 6 and similarly in claims 7-8, 15-17 and 22-25. As understood by the Applicants, the Examiner asserts that memory 110 of Moran inherently discloses a memory manager configured to determine susceptibility upon a request to allocate an additional page of RAM for the program. Applicants respectfully traverse the assertion that Moran inherently discloses the above-cited claim limitation. The Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that memory 110 of Moran inherently discloses a memory manager configured to determine susceptibility upon a request to allocate an additional page of RAM for the program. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). As the Examiner has not provided any objective evidence in supporting the assertion that Moran inherently discloses the above-cited claim limitation, the Examiner has not presented a *prima facie* case of anticipation for rejecting claims 6-8, 15-17 and 22-25. M.P.E.P. §2131.

Applicants further assert that Moran does not disclose "wherein the memory manager code comprises the process structure table code as an API" as recited in claims 13-14. As understood by the Applicants, the Examiner asserts that memory 110 of Moran inherently discloses the above-cited claim limitation. Applicants respectfully traverse the assertion that memory 110 of Moran inherently discloses memory manager code that includes a process structure table code as an API. The Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that memory 110 inherently discloses memory manager

code that comprises a process structure table code as an API. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). As the Examiner has not provided any objective evidence to support the assertion that memory 110 of Moran inherently discloses a memory manager code that comprises a process structure table code as an API, the Examiner has not presented a *prima facie* case of anticipation for rejecting claims 13-14. M.P.E.P. §2131.

As a result of the foregoing, Applicants respectfully assert that not each and every claim limitation was found within the cited prior art reference, and thus claims 1-25 are not anticipated by Moran.

II. CONCLUSION

As a result of the foregoing, it is asserted by Applicants that claims 1-25 in the Application are in condition for allowance, and Applicants respectfully request an allowance of such claims. Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining issues.

Respectfully submitted,

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